AMENDMENTS TO THE CLAIMS

The listing of claims below replaces all prior versions of claims in the application.

1. (Currently Amended) A semiconductor device comprising:

a gate formed over a semiconductor region while placing an insulating film in between;

a first impurity-diffused region formed, as being aligned with said gate, in the surficial layer of said semiconductor region;

a second impurity-diffused region formed, as being distant from said gate while placing a portion of a side of said first impurity-diffused region in between; and

a third impurity-diffused region formed, as being distant from said gate while placing said portion of said side of said first impurity-diffused region and a portion of a side of said second impurity-diffused region in between;

wherein said third impurity-diffused region has a higher impurity-concentration than said second impurity-diffused region;

wherein said second impurity-diffused region is formed as containing a diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region;

wherein said third impurity-diffused region is formed deeper than said second impurity-diffused region;

wherein said diffusion suppressive element is at least any one element selected from germanium, nitrogen, fluorine and carbon for the case where said impurity contained in said first and third impurity-diffused regions is an n-type impurity.

2. (Original) The semiconductor device according to claim 1, further comprising:

a first sidewall spacer formed over both lateral faces of said gate; and

a second sidewall spacer formed to cover said first sidewall spacer over both lateral sides of said gate;

wherein said second impurity-diffused region is formed as being aligned with said first sidewall spacer, and said third impurity-diffused region is formed as being aligned with said second sidewall spacer.

3. (Original) The semiconductor device according to claim 1, further comprising a fourth impurity-diffused region formed, in the surficial layer of said semiconductor region, as being aligned with said gate and as containing an impurity having a conductivity type opposite to that of impurities contained in said first and third impurity-diffused regions.

4-5. (Cancelled)

6. (Withdrawn) A method of fabricating a semiconductor device comprising the steps of:

forming a gate over a semiconductor region while placing an insulating film in between;

forming a first impurity-diffused region by introducing an impurity into a surficial layer of said semiconductor region under masking by said gate;

forming a first sidewall spacer over both lateral faces of said gate;

forming an amorphous second impurity-diffused region by introducing a diffusion suppressive element into the surficial layer of said semiconductor region under masking by said gate and said first sidewall spacer;

forming a second sidewall spacer to cover said first sidewall spacer over both lateral sides of said gate; and

forming a third impurity-diffused region by introducing an impurity into the surficial layer of said semiconductor region to a depth larger than that of said first impurity-diffused region under masking by said gate, said first sidewall spacer and said second sidewall spacer.

7. (Withdrawn) The method of fabricating a semiconductor device according to claim 6, further comprising a step of forming a fourth impurity-diffused region by introducing an impurity, having a conductivity type opposite to that of the impurities contained in said first and third impurity-diffused regions, into the surficial layer of said semiconductor region under masking by said gate and said first sidewall spacer.

8. (Withdrawn) The method of fabricating a semiconductor device according to claim 6, wherein said diffusion suppressive element is at least any one element selected from arsenic,

germanium, nitrogen, fluorine and carbon for the case where said impurity contained in said first and third impurity-diffused regions is an n-type impurity.

9. (Withdrawn) The method of fabricating a semiconductor device according to claim 6, wherein said diffusion suppressive element is at least any one element selected from germanium, nitrogen, fluorine, carbon and indium for the case where said impurity contained in said first and third impurity-diffused regions is a p-type impurity.

10. (Withdrawn) The method of fabricating a semiconductor device according to claim 6, wherein said first sidewall spacer is formed at a first temperature using a material formed at said first temperature not causative of activation of said impurity contained in said first impurity-diffused region.

11. (Withdrawn) The method of fabricating a semiconductor device according to claim 10, wherein said first temperature falls within a range from 500°C to 580°C.

12. (Withdrawn) The method of fabricating a semiconductor device according to claim 6, wherein said second sidewall spacer is formed at a second temperature using a material formed at said second temperature not causative of re-crystallization of said second impurity-diffused region.

13. (Withdrawn) The method of fabricating a semiconductor device according to claim 12, wherein said second temperature falls within a range from 500°C to 580°C.

14. (Previously Presented) The semiconductor device according to claim 1, wherein said third impurity-diffused region has a higher impurity-concentration than said first impurity-diffused region

15. (Currently Amended) A semiconductor device comprising:

a gate formed over a semiconductor region while placing an insulating film in between;

a first impurity-diffused region formed, as being aligned with said gate, in the surficial layer of said semiconductor region;

a second impurity-diffused region formed, as being distant from said gate while placing a portion of a side of said first impurity-diffused region in between; and

a third impurity-diffused region formed, as being distant from said gate while placing said portion of said side of said first impurity-diffused region and a portion of a side of said second impurity-diffused region in between;

wherein said third impurity-diffused region has a higher impurity-concentration than said second impurity-diffused region;

wherein said second impurity-diffused region is formed as containing a diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region;

wherein said diffusion suppressive element is at least any one element selected from ~~arsenic,~~ germanium, nitrogen, fluorine and carbon for the case where said impurity contained in said first and third impurity-diffused regions is an n-type impurity.

16. (Previously Presented) The semiconductor device according to claim 15, further comprising:

a first sidewall spacer formed over both lateral faces of said gate; and

a second sidewall spacer formed to cover said first sidewall spacer over both lateral sides of said gate;

wherein said second impurity-diffused region is formed as being aligned with said first sidewall spacer, and said third impurity-diffused region is formed as being aligned with said second sidewall spacer.

17. (Previously Presented) The semiconductor device according to claim 15, further comprising a fourth impurity-diffused region formed, in the surficial layer of said semiconductor region, as being aligned with said gate and as containing an impurity having a conductivity type opposite to that of impurities contained in said first and third impurity-diffused regions.

18. (Previously Presented) The semiconductor device according to claim 15, wherein said diffusion suppressive element is at least any one element selected from germanium, nitrogen,

fluorine, carbon and indium for the case where said impurity contained in said first and third impurity-diffused regions is a p-type impurity.

19. (Previously Presented) The semiconductor device according to claim 15, wherein said third impurity-diffused region has a higher impurity-concentration than said first impurity-diffused region

20. (Currently Amended) A semiconductor device comprising:

a gate formed over a semiconductor region while placing an insulating film in between;

a first impurity-diffused region formed, as being aligned with said gate, in the surficial layer of said semiconductor region;

a second impurity-diffused region formed, as being distant from said gate while placing a portion of a side of said first impurity-diffused region in between; and

a third impurity-diffused region formed, as being distant from said gate while placing said portion of said side of said first impurity-diffused region and a portion of a side of said second impurity-diffused region in between;

wherein said third impurity-diffused region has a higher impurity-concentration than said second impurity-diffused region;

wherein said second impurity-diffused region is formed as containing a diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region;

wherein said diffusion suppressive element is at least any one element selected from germanium, nitrogen, fluorine[[,]] and carbon ~~and indium~~ for the case where said impurity contained in said first and third impurity-diffused regions is a p-type impurity.

21. (Previously Presented) The semiconductor device according to claim 20, further comprising:

a first sidewall spacer formed over both lateral faces of said gate; and

a second sidewall spacer formed to cover said first sidewall spacer over both lateral sides of said gate;

wherein said second impurity-diffused region is formed as being aligned with said first sidewall spacer, and said third impurity-diffused region is formed as being aligned with said second sidewall spacer.

22. (Previously Presented) The semiconductor device according to claim 20, further comprising a fourth impurity-diffused region formed, in the surficial layer of said semiconductor region, as being aligned with said gate and as containing an impurity having a conductivity type opposite to that of impurities contained in said first and third impurity-diffused regions.

23. (Previously Presented) The semiconductor device according to claim 20, wherein said diffusion suppressive element is at least any one element selected from arsenic, germanium,

nitrogen, fluorine and carbon for the case where said impurity contained in said first and third impurity-diffused regions is an n-type impurity.

24. (Previously Presented) The semiconductor device according to claim 20, wherein said third impurity-diffused region has a higher impurity-concentration than said first impurity-diffused region.

25. (New) A semiconductor device comprising:

a gate formed over a semiconductor region while placing an insulating film in between;

a first impurity-diffused region formed, as being aligned with said gate, in the surficial layer of said semiconductor region;

a second impurity-diffused region formed, as being distant from said gate while placing a portion of a side of said first impurity-diffused region in between; and

a third impurity-diffused region formed, as being distant from said gate while placing said portion of said side of said first impurity-diffused region and a portion of a side of said second impurity-diffused region in between;

wherein said third impurity-diffused region has a higher impurity-concentration than said second impurity-diffused region;

wherein said second impurity-diffused region is formed as containing a diffusion suppressive element for suppressing diffusion of an impurity contained in said third impurity-diffused region;

wherein said third impurity-diffused region is formed deeper than said second impurity-diffused region;

wherein said diffusion suppressive element is at least any one element selected from germanium, nitrogen, fluorine, and carbon for the case where said impurity contained in said first and third impurity-diffused regions is a p-type impurity.

26. (New) The semiconductor device according to claim 25, further comprising:

a first sidewall spacer formed over both lateral faces of said gate; and

a second sidewall spacer formed to cover said first sidewall spacer over both lateral sides of said gate;

wherein said second impurity-diffused region is formed as being aligned with said first sidewall spacer, and said third impurity-diffused region is formed as being aligned with said second sidewall spacer.

27. (New) The semiconductor device according to claim 25, further comprising a fourth impurity-diffused region formed, in the surficial layer of said semiconductor region, as being aligned with said gate and as containing an impurity having a conductivity type opposite to that of impurities contained in said first and third impurity-diffused regions.

28. (New) The semiconductor device according to claim 25, wherein said third impurity-diffused region has a higher impurity-concentration than said first impurity-diffused region.